METHOD AND APPARATUS FOR OPTIMIZING THE TIMING OF INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

Integrated circuits are designed having optimal signal timing between and among cells. A set of identities are generated corresponding to logic operations and to library cells in technology basis. A resynthesis window is created for the identities having less than a predetermined depth of critical variables. Logic equations of the resynthesis window are transformed using the identities, and the resynthesized window area is optimized.